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(REV. 2-92)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

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2304

ATTACHMENT
TO
PAPER
NUMBER

3

NOTICE OF REFERENCES CITED

APPLICANT(S)

Jack D. Pippin

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
A		4 7 7 9 1 6 1	10/18/88	DeShazo, Jr.	361	106	
B		4 7 8 7 0 0 7	11/22/88	Matsumura et al.	361	98	
C		4 7 8 9 8 1 9	12/6/88	Nelson	323	314	
D		4 9 0 3 1 0 6	2/20/90	Fukunaga et al.	357	43	
E		4 9 3 5 8 6 4	6/19/90	Schmidt et al.	363	141	
F		5 0 8 7 8 7 0	2/11/92	Salesky et al.	323	276	
G		5 1 4 9 1 9 9	9/22/92	Kinoshita et al.	374	178	
H		5 1 7 0 3 4 4	12/8/92	Berton et al.	364	400	
I		5 2 8 3 6 3 1	2/11/94	Koerner et al.	307	451	
J		5 3 2 5 2 8 6	6/28/94	Weng et al.	364	557	
K		5 3 5 9 2 3 6	10/25/94	Giordano et al.	307	310	

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*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
L									
M									
N									
O									
P									
Q									

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	Allen and Holbag, "CMOS Analog Circuit Design," HRW, pp. 539-549, 1987
S	
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EXAMINER

Thai Phan

DATE

3/28/95

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)